ADVANCED

GT23SC4428

1-KBYTE EEPROM
WITH WRITE PROTECT FUNCTION AND PROGRAMMABLE SECURITY CODE

Table of Content

1 FEATURES

- Standard CMOS process
- 1024 x 8 bits EEPROM organization
- Byte-wise addressing
- Byte-wise erase/write
- Irreversible byte-wise write protection
- Single 5V power supply for read and write/erase
- Low power operation:
  - 3 mA typical active current
- 5 ms programming time
- 3-wire serial interface
- 20 KHz serial clock rate
- Contact configuration and serial interface, ISO standard 7816 (Synchronous Transmission) compatible.
- High ESD protection: > 4 KV
- High reliability:
  - 1,000,000 erase/write cycles guaranteed
  - 10 years data retention
- Wide operating temperature range

  – 0 to +70°C Commercial; –40 to +85°C Industrial
- 2-byte Programmable Security Code (PSC) for memory write/erase protection

2 DESCRIPTION

GT23SC4428 contains 1024 x 8 bits of EEPROM with programmable write protection for each byte. Random read access to any byte in the memory is always possible. The memory can also be erased and written byte by byte. Erasing old data in the byte location must be performed before new data can be written to the location. Each byte in the memory has a corresponding protect bit. The protect bits are only one-time programmable and cannot be erased. After the protect bits are enabled (logic 0), the corresponding bytes can never be changed again. A write-protect bit with data-compare function is available for user to verify the data in the memory before enabling the protect bit.

In addition, it offers two bytes of Programmable Security Code (PSC) against unauthorized memory write/erase operations. All the memory, except for the PSC can always be read, but the memory can be written or erased only after PSC verification. If the user fails to enter the correct PSC in eight consecutive attempts, the device will block any further PSC entry attempts and the memory can never be erased or written again.

The PSC bytes are pre-programmed by the manufacturer with a code, which is specified for the customer for device transport security purposes, before the devices are shipped to the customer. The Error Counter will be pre-erased by the manufacturer to allow maximum attempts (maximum of eight) for PSC entry.

3 BLOCK DIGRAM

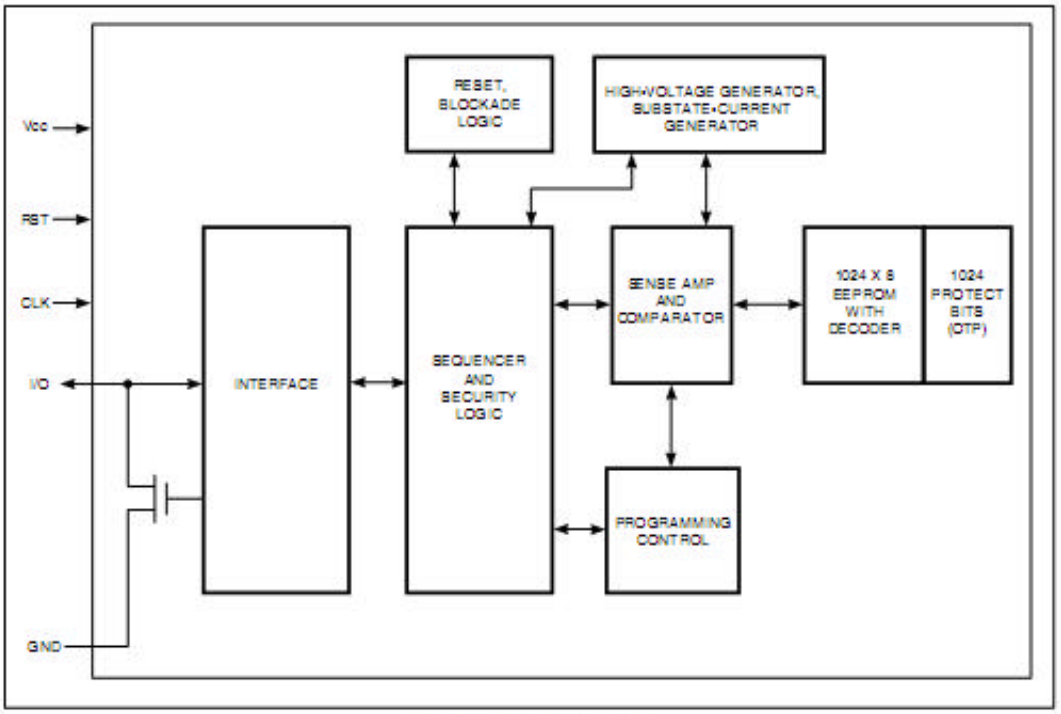
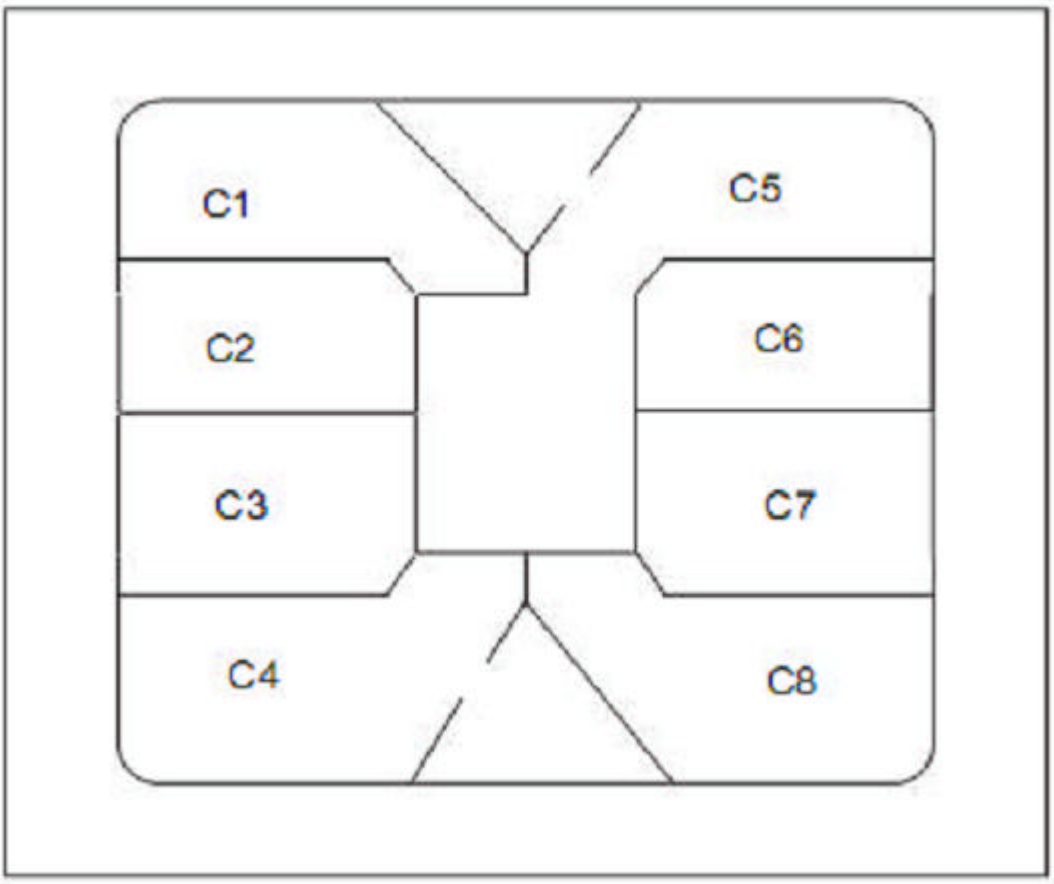


Figure 1. Block Diagram

4 PIN CONFIGURATION



PIN NAMES

Pin	Card Contact	Symbol	Description
1	C1	Vcc	Supply Voltage
2	C2	RST	Reset
3	C3	CLK	Serial Clock
4	C4	NC	No Connect
5	C5	GND	Ground
6	C6	NC	No Connect
7	C7	I/O	Serial Data I/O (open drain)
8	C8	NC	No Connect

PIN DESCRIPTIONS

Symbol	Type	Card Contact	Name and Function
Vcc		C1	Supply Voltage
RST		C2	Reset: The device reset pin (RST) is used to take the device out of the power-on reset state (POR). When the operating power is first applied to Vcc, the device goes into POR state. The POR state can be terminated by RST in this sequence: bring RST from 0 to 1 and then change CLK from 0 to 1 (See Figure 3). This reset operation terminates any active command operation. After the POR state has been terminated, a read operation must be performed before any data can be erased or written. Also, GT23SC4418/28 meets the ISO 7816 specification on Answer to Reset function. The Answer to Reset can be invoked by performing the following steps: 1) RST goes from 0 to 1; 2) CLK pulse is applied; 3) RST changes from 1 to 0. If these steps are performed correctly, the device will set the address counter to 0 and the first data bit at byte address 0 will appear on the output (I/O). By continuing to send pulses at CLK, the contents of the following byte addresses can be read out of the device. (See Figure 3) In normal

operation, RST controls the data input and output directions. When sending data/command to the device, RST is set to 1. When reading data/PSC verification output from the device, RST is set to 0. (See Figure 4)

CLK	C3	**Serial Clock:** This is the device data clock pin. It is used to clock data bits into and out of the device.
NC	C4, C6, C8	**No Connect**
GND	C5	**Ground**
I/O	C7	**Serial Data Input and Output:** This pin is where data is shifted in and out of the device.

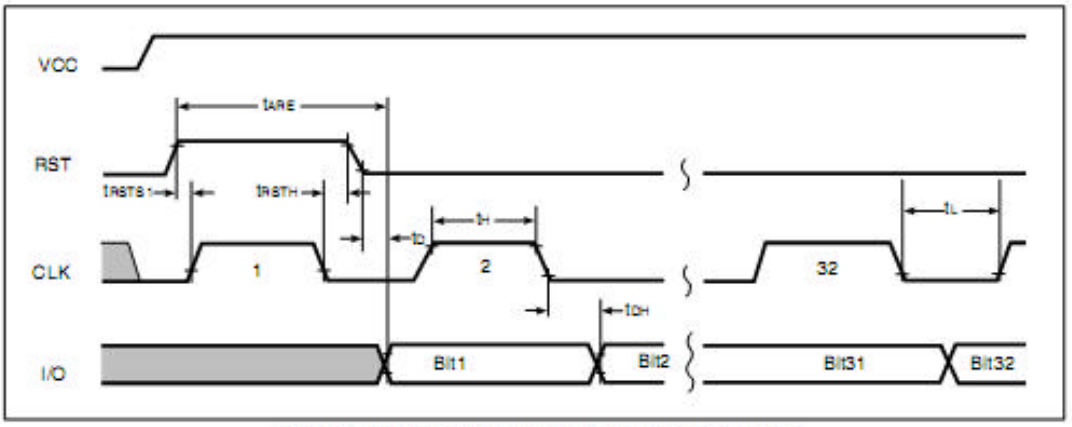


Figure 3. Reset and Answer to Reset Timing Diagram

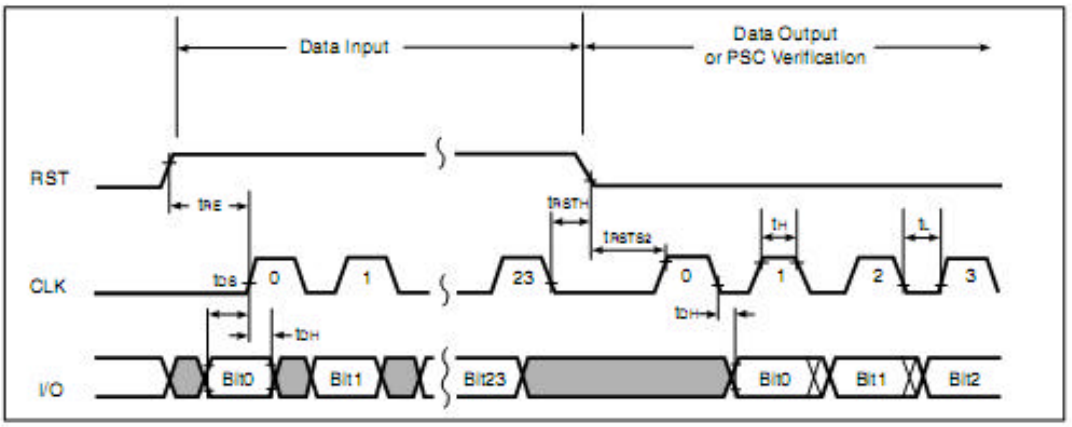


Figure 4. General Timing for Data Input, Data Output and PSC Verification

5 GENERAL COMMAND DESCRIPTIONS

Table 1. Control Words for IS23SC4418/4428 Commands

Command Name	Byte 1							Byte 2	Byte 3
	S0	S1	S2	S3	S4	S5	A8 A9	A0-A7	D0-D7
Read 8-bits data without protect bit	0	1	1	1	0	0	A8 A9	A0-A7	Don't Care
Read 9-bits data with protect bit	0	0	1	1	0	0	A8 A9	A0-A7	Don't Care
Write and erase without protect bit(1)	1	1	0	0	1	1	A8 A9	A0-A7	Input data
Write and erase with protect bit(1)	1	0	0	0	1	1	A8 A9	A0-A7	Input data
Write protect bit with data comparison(1)	0	0	0	0	1	1	A8 A9	A0-A7	Compare data

Additional Commands for IS23SC4428 only(3)

Additional Commands for IS23SC4428 only(3)									
Write Error Counter	0	1	0	0	1	1	1	1	FDH	Bit Mask
Verify first PSC byte	1	0	1	1	0	0	1	1	FEH	PSC byte 1
Verify second PSC byte	1	0	1	1	0	0	1	1	FFH	PSC byte 2
Write and erase first PSC byte without protect bit(2)	1	1	0	0	1	1	1	1	FEH	PSC byte 1
Write and erase second PSC byte without protect bit(2)	1	1	0	0	1	1	1	1	FFH	PSC byte 2
Write and erase first PSC byte with protect bit(2)	1	0	0	0	1	1	1	1	FEH	PSC byte 1
Write and erase second PSC byte with protect bit(2)	1	0	0	0	1	1	1	1	FFH	PSC byte 2
Read 8-bits first PSC byte without protect bit(2)	0	1	1	1	0	0	1	1	FEH	Don't Care
Read 8-bits second PSC byte without protect bit	0	1	1	1	0	0	1	1	FFH	Don't Care
Read 9-bits first PSC byte with protect bit	0	0	1	1	0	0	1	1	FEH	Don't Care
Read 9-bits second PSC byte with protect bit	0	0	1	1	0	0	1	1	FFH	Don't Care

Notes:

1. If the protect bit of the byte address is enabled, the write command will have no effect on the byte content.

2. If the protect bit of the PSC byte is enabled, the write command will have no effect on the PSC byte.

3. For IS23SC4428, locations (1021-1023) are occupied by Error Counter and PSC codes and thus cannot be used for general data storage.

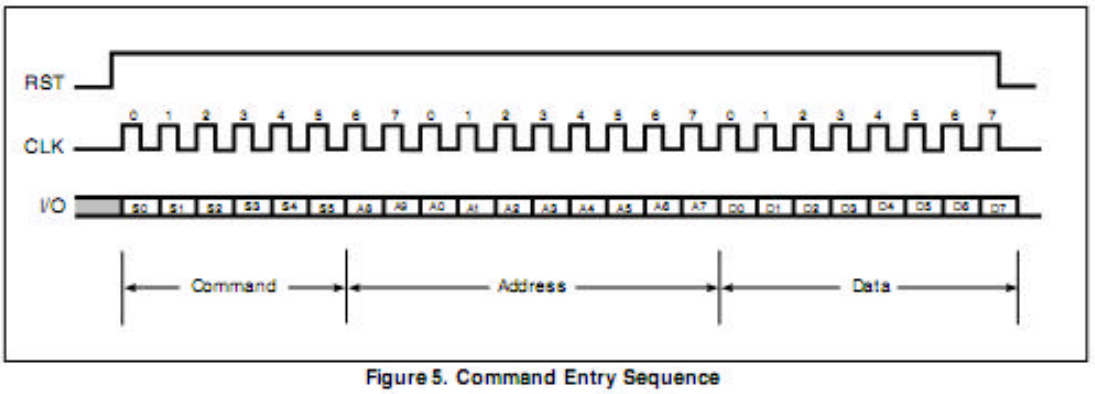


Figure 5. Command Entry Sequence

Read 8-Bits Data

The read 8-bit data command allows the user to specify the address (A0-A9) of the data byte to be read from the device. The byte address for the next output data is automatically incremented after every eight clock pulses. The data is output in sequential order, with the data from address n followed by the data from address n+1. (See Figure 6.)

Read 9-Bits Data with Protect Bit

The read 9-bit data command operates similarly to read 8-bit data command except that the protect bit for each byte is output after each 8-bit data and the address for the next output data is incremented after every nine clock pulses. (See Figure 7.)

Write/Erase Data Byte without Protect Bit

The write/erase data byte without protect bit command writes the new data into the specified byte location. There are three kinds of write/erase operations which are automatically executed by the device:

1. Erase and subsequent write if 203 clock pulses at f < 20 KHz are applied. (See Figure 8.)

2. Write only if 103 clock pulses at f < 20 KHz are applied. This operation is only suitable if single bits of one byte shall be changed only from 1 to 0. (See Figure 9.)

3. Erase only if the input data = FFH and 103 clock pulses at f < 20 KHz are applied. (See Figure 9.)

Note: Erase means 0 → 1. Write means 1 → 0.

If the protect bit of the corresponding byte location is enabled, the write/erase operation will have no effect on the content.

Write/Erase Data Byte with Protect Bit

The write/erase data byte with protect bit command operates similarly to the write/erase data bytewith protect bit command except that it also writes 0 to the corresponding protect bit. After the protect bit is set to 0 (write protection enabled), it cannot be changed again. (See Figures 8 and 9.)

Write Protect Bit with Data Comparison

The write protect bit with data comparison command writes 0 to the corresponding protect bit only if the input data and the data in the specified memory location are the same. After the protect bit is set to 0 (write protection enabled), it cannot be changed again. (See Figure 9.)

The execution of write/erase commands are terminated after a given number of clock cycles. When the operation is done, the device will bring the I/O state to 0. Only RST transition from 0 to 1 can set the I/O state back to 1.

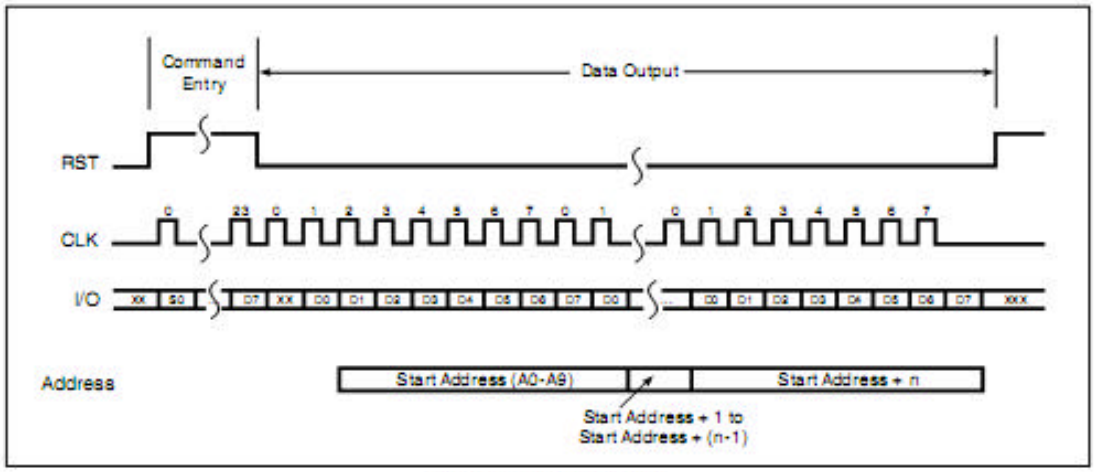


Figure 6. Read 8-bit Data

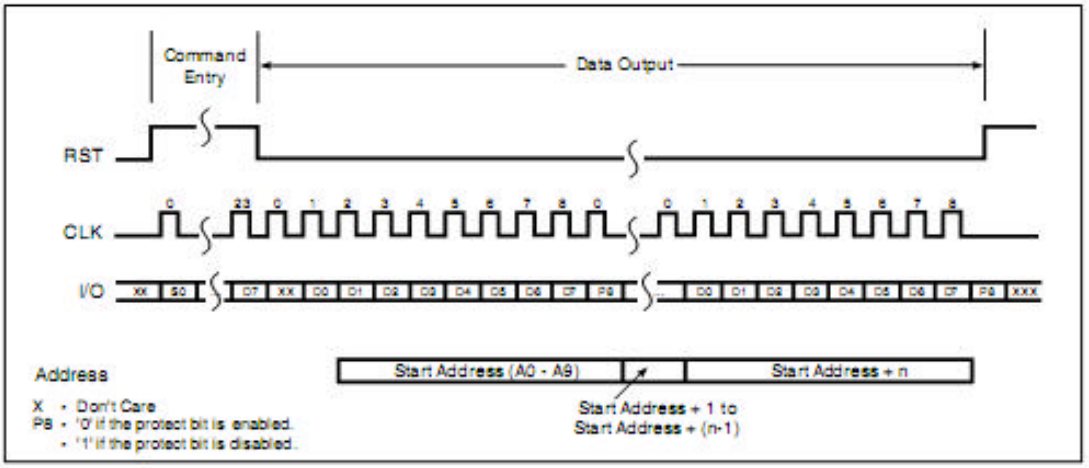


Figure 7. Read 9-bit Data with Protect Bit

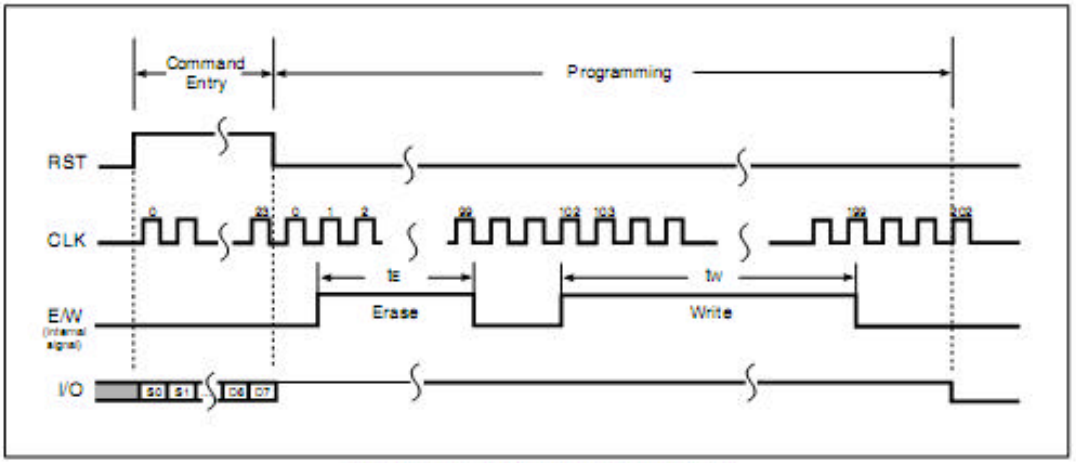


Figure 8. Programming Erase and Write

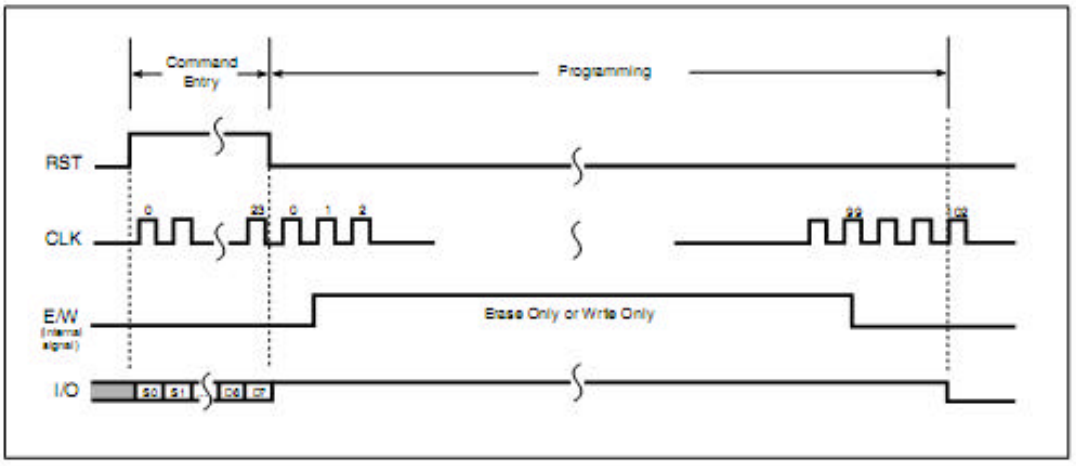


Figure 9. Programming Erase Only or Write Only

6 GT23SC4428 SECURITY FEATURES

Overview

Without entering Programmable Security Code (PSC), only memory read access is possible. However, the content of the PSC addresses (1022 and 1023) cannot be read out. If reading PSC is attempted, 00H will be output. The PSC verification procedure must be performed in the following sequence:

1. Write one to not-written Error Counter bit, address 1021

2. Enter first PSC byte, address 1022

3. Enter second PSC byte, address 1023

4. After successful PSC verification, the Error Counter should be erased to reactivate the 8 PSC entry attempts. If the PSC entry is incorrect, go back to step 1. If all the Error Counter bits have been written, any further PSC entry will be blocked and the memory can never be changed again.

Writing Error Counter

The number of erased bits (logic 1) in Error Counter determines the number of possible attempts (maximum of eight). Before PSC entry, only writing of error counter is possible. After PSC is successfully verified, the counter can now be erased. Before disconnecting the supply voltage Vcc, the counter should be erased in order to reactivate the eight attempts. (See Figure 10.)

Entry of PSC

The least significant PSC byte beginning with the least significant bit must be entered first and then the most significant (see Table 1). If both PSC byte 1's and byte 2's comparisons prove correct, the memory erase/write access will be enabled and PSC may be changed as wished, except the corresponding protect bits are 0 (enabled). (See Figure 11.)

Condition when supplied

GT23SC4428 is supplied by the manufacturer with a 2byte PSC (transport security code) which is determined in cooperation with the customer.

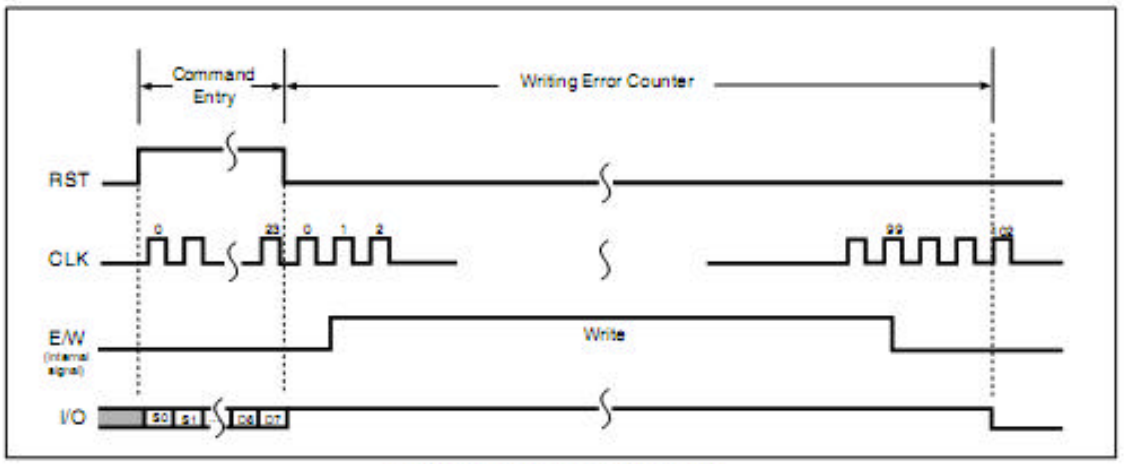


Figure 10. Writing Error Counter

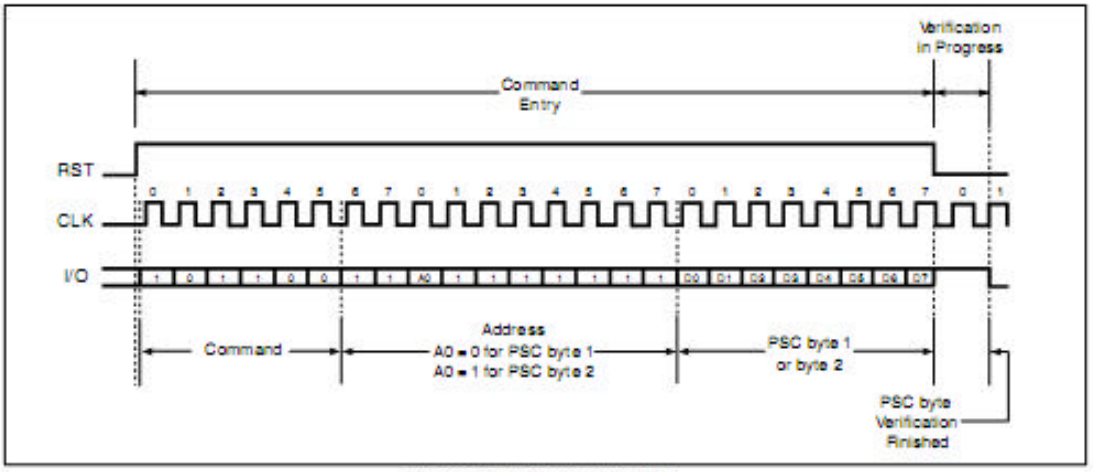


Figure 11. PSC Verification

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7 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	–0.3	6	V
VI	Input Voltage	–0.3	6	V
T_{STG}	Storage Temperature	–40	125	°C
P_{MAX}	Power Dissipation	—	60	mV

CAPACITANCE (T_A = 25°C, V_{CC} = 5.0V ± 10%, f = 1 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

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DC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
I_{CC}	Supply Current		—	3	10	mA
V_{IH}	Input HIGH Voltage (I/O, CLK, RST)		3.5	—	5.0	V
V_{IL}	Input LOW Voltage (I/O, CLK, RST)		0	—	0.8	V
I_{IH}	Input HIGH Current (I/O, CLK, RST)		—	—	10	µA
I_{OL}	Output LOW Current	V_{OL} = 0.4V, open drian	0.5	—	—	mA
I_{OH}	output HIGH Leakage Current	V_{OH} = 5V, open drian	—	—	10	µA

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
fc	Clock Frequency		—	20	—	KHz
t_{RE}	Reset Time		9	—	—	µs
t_{ARE}	Answer to Reset		20	50	—	µs
t_H	Clock HIGH Period		10	—	—	µs
t_L	Clock LOW Period		10	—	—	µs
tw	Write Time	(fc = 20 KHz)	5	—	—	ms
te	Erase Time	(fc = 20 KHz)	5	—	—	ms
t_{RSTS1}	Reset Setup Time 1		4	—	—	µs
t_{RSTS2}	Reset Setup Time 2		4	—	—	µs
t_{RSTH}	Reset Hold Time		4	—	—	µs
tos	Write Data Setup Time		4	—	—	µs
toH	Write Data Hold Time		4	—	—	µs
to	Read Data Delay Time		6	—	—	µs
tR	Rise Time (I/O, CLK, RST)		—	—	1	µs
tF	Fall Time (I/O, CLK, RST)		—	—	1	µs

8 REVISION HISTORY

Revision	Date	Descriptions
a0	Mar 2010	Initial version